

INTEGRATION AND HOLD PHASE DETECTION

Abstract of the Disclosure

5 The invention relates to methods and apparatus that allow a comparison of phase between a clock signal and a serial bitstream. A phase detector integrates a portion of a transition between adjacent or consecutive bits of the serial bitstream in a relatively fixed window. Advantageously, the relatively fixed window permits operation at relatively high frequencies such as at OC-192 rates of SONET. The integration result contains an amount of time within the window spent in one logic state versus the other. The integration results are held until the logic levels of the integrated bits are ascertained. An indication of a logic level transition is used to relate the integration result to the timing of the transition within the integration window. Multiple bit transitions can be integrated, correlated to timing information, summed, and provided as an input to, for example, a voltage controlled oscillator in a phase-locked loop.

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